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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,751	04/13/2001	Sergey A. Velichko	303.750US1	4280
21186	7590	10/28/2003	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			MILLER, CRAIG S	
			ART UNIT	PAPER NUMBER
			2857	

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

89/834,751

Applicant(s)

Velichko et al.

Examiner

CRAIG STEVEN M. HEN

Group Art Unit

2857

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- ☒ Responsive to communication(s) filed on 15 Oct 2001
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 1-58 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1-58 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).
- ☐ All ☐ Some* ☐ None of the:
- ☐ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. _____.
- ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____

Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
- ☒ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Interview Summary, PTO-413
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Other _____

Office Action Summary

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

*A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

2. Claims 1, 2, 4-9, 16-22, 29, 30 and 32-37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ekstedt *et al.* (5,206,582).

As to claims 1, 2, 6-9, 16, 19-22, 29, 30, 34-37, 44, 45 and 49-52, Ekstedt *et al.* discloses a control module (fig. 8 and [16]) to control concurrently operation of the semiconductor test equipment and operation of parametric test instrumentation (functional block [76] of fig. 9).

As to claims 4, 5, 17, 18, 32, 33, 47 and 48 Ekstedt *et al.* discloses a prober [13] and parametric measurement instruments [10].

More particularly with respect to claims 44, 45 and 47-52, said claims are directed towards computer (machine) readable media. Because the functions of Ekstedt *et al.* are disclosed as being computer implemented, particularly with a general test computer program (fig. 2), it is deemed inherent that such computer programs shall reside upon computer readable media such as fixed disk harddrives.

3. The following is a quotation of 35 U.S.C. § 103 (b) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Should it be determined by competent authority that the embedding of the computer (machine) programs of Ekstedt *et al.* as applied within the rejections of claims 44, 45 and 47-52 above is not inherent, their inclusion within the rejections below under U.S.C. § 103 is deemed appropriate.

5. Claims 3, 10-15, 23-28, 31 and 38-43, 46 and 53-58 are rejected under 35 U.S.C. § 103(b) as being unpatentable over Ekstedt *et al.*

As to claims 44, 45 and 49-52, Ekstedt *et al.* discloses a control module (fig. 8 and [16]) to control concurrently operation of the semiconductor test equipment and operation of parametric test instrumentation (functional block [76] of fig. 9). Ekstedt *et al.* does not specify that the disclosed functions should be embodied within a computer (machine) readable medium. Because the functions of Ekstedt *et al.* are disclosed as being computer implemented and because it is well known that such computer functions are implemented via computer readable code and because it is well known that such code is commonly embodied upon computer readable media, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the computer functions of Ekstedt *et al.* should be embodied upon computer readable media so as to receive the expected benefits derived there from such as enhanced system flexibility.

As to claims 47 and 48, Ekstedt *et al.* discloses a prober [13] and parametric measurement instruments [10].

As to claims 3, 31 and 46, said claims are directed towards implementing the control functions within electronic hardware. The use of electronic hardware is well known within the IC test arts for testing circuits. Programmed hardware implementing test functions are well known functional equivalents to software implemented test functions and are often used when changes in test programs are not of main concern. Therefore, because Ekstedt *et al.* does not preclude the performance of the test functions within pre-programmed electronic hardware and because Applicants fails to claim any particular unexpected result or synergistic effect from such use, it would have been obvious to one of ordinary skill in the art at the time the invention was made that pre-programmed electronic hardware could be substituted for the software programmable functions of Ekstedt *et al.*, each performing similar functions in similar ways, so as to receive the expected benefits derived there from such as enhanced system reliability.

As to claims 10, 11, 13-15, 23, 24, 26-28, 38, 39, 41-43, 53, 54 and 56-58, said claims are directed towards the control module controlling the test state via a state oscillator module controlling other modules. Ekstedt *et al.* as modified above discloses the instant invention with the exception that

Ekstedt *et al.* as modified above does not specify that the control module synchronously sets the test state through a state oscillator module. Ekstedt *et al.* discloses in col. 4 that any appropriate test may be performed by the invention. The Examiner takes notice that parametric testing of ICs is commonly performed with clock synchronization of test modules, including the control module to minimize measurement faults and that oscillators are a well known and conventional producer of such clock signals. The Examiner further takes note that there is no invention in shifting the location of elements within a device unless there exists an unexpected result or synergistic effect from any particular claimed location. Therefore, because Ekstedt *et al.* discloses the use of generic parametric tests, because such tests are well known to include synchronous elements and because the control source of the synchronizing signal may be shifted, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Ekstedt *et al.*, as modified above, a known synchronous control signal from the control module through a conventional synchronous clock signal source to test implementation modules so as to receive the expected results expected there from, such as increased test reliability.

Furthermore with respect to claim 13, 26, 41 and 56, Ekstedt *et al.* as modified above discloses the instant invention with the exception that Ekstedt *et al.* as modified above does not specify that the state oscillator module controls other modules during conventional operational superstates. Ekstedt *et al.* discloses in col. 4 that any appropriate test may be performed by the invention. The Examiner further takes note that there is no invention in shifting the location of elements within a device unless there exists an unexpected result or synergistic effect from any particular claimed location. Therefore, because Ekstedt *et al.* as modified above discloses the use of synchronous control, because conventional test superstates such as abort, pause, etc. require such synchronicity and because the control source of the synchronizing signal may be shifted, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Ekstedt *et al.*, as modified above, that the state oscillator module controls other modules during conventional operational superstates so as to receive the expected results expected there from, such as increased test reliability.

As to claims 12, 25, 40 and 55, said claims are directed towards the control module controlling the state oscillator module and other modules. Ekstedt *et al.* as modified above discloses the instant invention with the exception that Ekstedt *et al.* as modified above does not specify that the control module synchronously sets the state oscillator module and other test modules. Ekstedt *et al.* discloses in col. 4 that any appropriate test may be performed by the invention. The Examiner takes notice that parametric testing of ICs is commonly performed with clock synchronization of test modules, including the control module to minimize measurement faults and that oscillators are a well known and conventional producer of such clock signals and that a control unit may control the oscillator and associated other test modules. The Examiner further takes note that there is no invention in shifting the location of elements within a device unless there exists an unexpected result or synergistic effect from any particular claimed location. Therefore, because Ekstedt *et al.* discloses the use of generic parametric tests, because such tests are well known to include synchronous elements and because the control source of the synchronizing signal may be shifted, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Ekstedt *et al.*, as modified above, the control module synchronously controlling a state oscillator and associated test implementation modules so as to receive the expected results expected there from, such as increased test repeatability.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chiu *et al.* (4,639,664) discloses testing circuits in parallel.

Jackson (4,656,632) discloses automated circuit testing. Jackson discloses in col. 5 that test synchronization is required in parametric testing.

Littlebury (4,985,988) discloses testing ICs.

Tsiang *et al.* (5,822,717) discloses wafer testing.

Testa *et al.* (5,845,234) discloses generation of automated test equipment program code.

Nakaizumi (6,031,382) discloses testing ICs.

Hauptman (6,331,783 B1) discloses automated test equipment.

Rohrbaugh *et al.* (6,556,938 B1) discloses automated test equipment.

Cheng *et al.* (6,590,408 B1) discloses electrical test equipment.

Takao (US 2002/0000826 A1) discloses semiconductor automated parametric testing.

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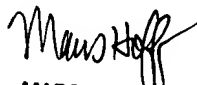
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7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Craig Steven Miller whose telephone number is (703) 305-9730. Art Unit facsimile services are now available at (703) 308-7722.

The Examiner can normally be reached on Mondays through Fridays from 07:30am-4:00pm EST. Should repeated attempts to reach the Examiner be unsuccessful, the Examiner's Supervisor, Marc Hoff may be reached at (703) 308-1677.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Craig Steven Miller (ss)
16 October 2003


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800